ECEN 325 - 516

Final Project:
Preliminary Report

Abin Antony

Mostak Ahmed

TA: Amir Tofighi

Date: 04/15/2019

Objective

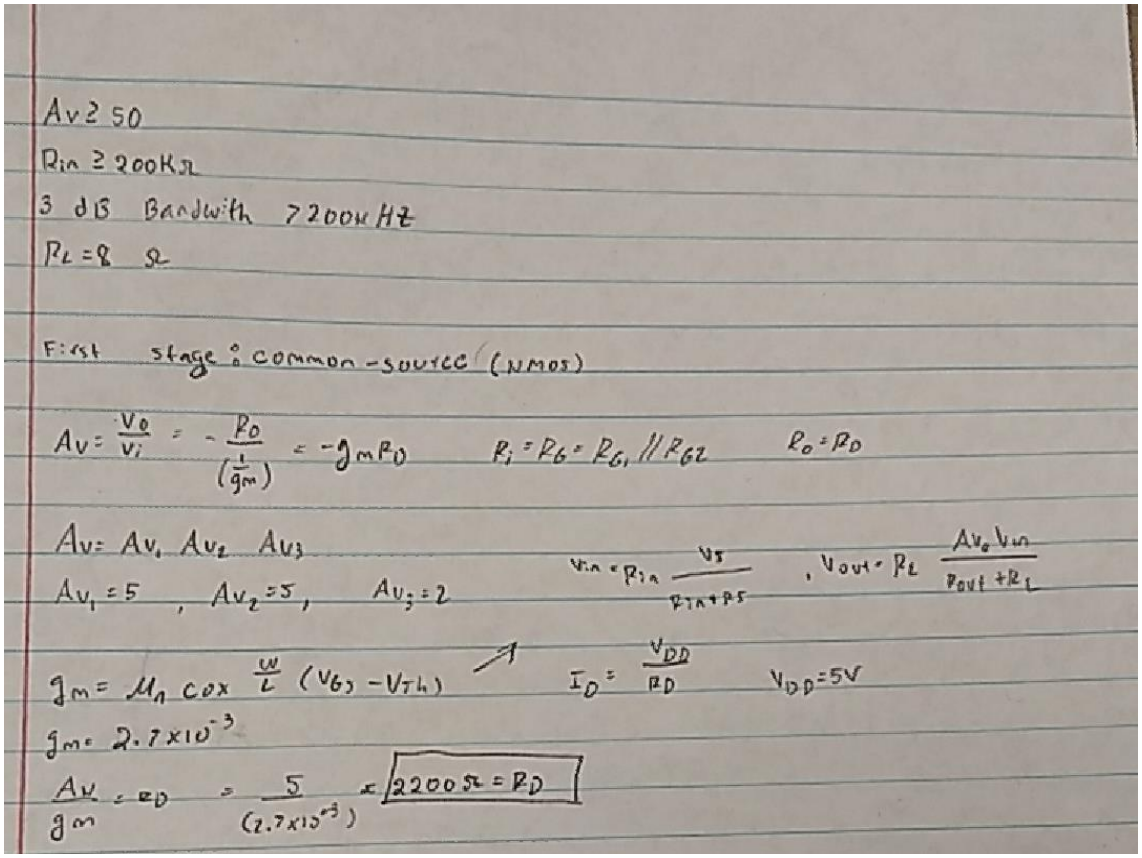
The objective of this project is to design a three-stage amplifier using bipolar and CMOS transistors. The design should satisfy the following specifications.

- $A_V \geq 50$
- $R_{in} \geq 200k\Omega$
- 3 dB Bandwidth > 200 kHz
- Harmonic distribution < -30dB
- $V_{imax} = 5mV_{PP}$
- $V_{cc,max} = 5V$
- $R_{Load} = 8\Omega$
- Minimum of 3 MOSFETs

Design

We designed the 3-stage amplifier using 3 common source MOSFET configuration stages. We designed the third stage in such a way that it gives a gain of 2 and the first two stages gives a gain of 5 each, providing the total gain, $A_V = A_{V1}A_{V2}A_{V3} = 5 \times 5 \times 2 = 25$.

Calculations



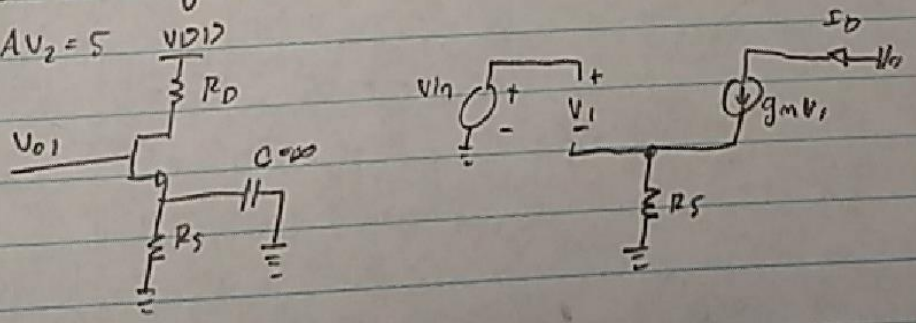
$R_D = R_D$ $\boxed{R_D = 2200\Omega}$

$R_{in} = 200K\Omega = R_{Gk} = R_{G1} // R_{G2} = (400K\Omega) // (400K\Omega) = \boxed{200K\Omega}$

$= R_{G1} = R_{G2}$

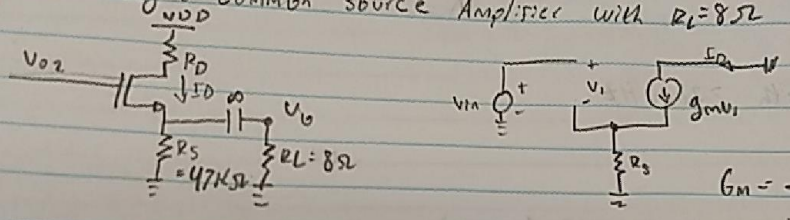
Second stage: common-source (NMOS) R_D, R_S, with source Degeneration

$A_{V_2} = 5$



$A_V = -\frac{g_m R_D}{1 + g_m R_S}$ $\quad A_V = 5 = \frac{(5.55 \times 10^{-5}) R_D}{1 + (5.55 \times 10^{-5})(22K)}$ $\quad \boxed{R_D = 20K\Omega}$

Third stage: common source Amplifier with $R_L = 8\Omega$



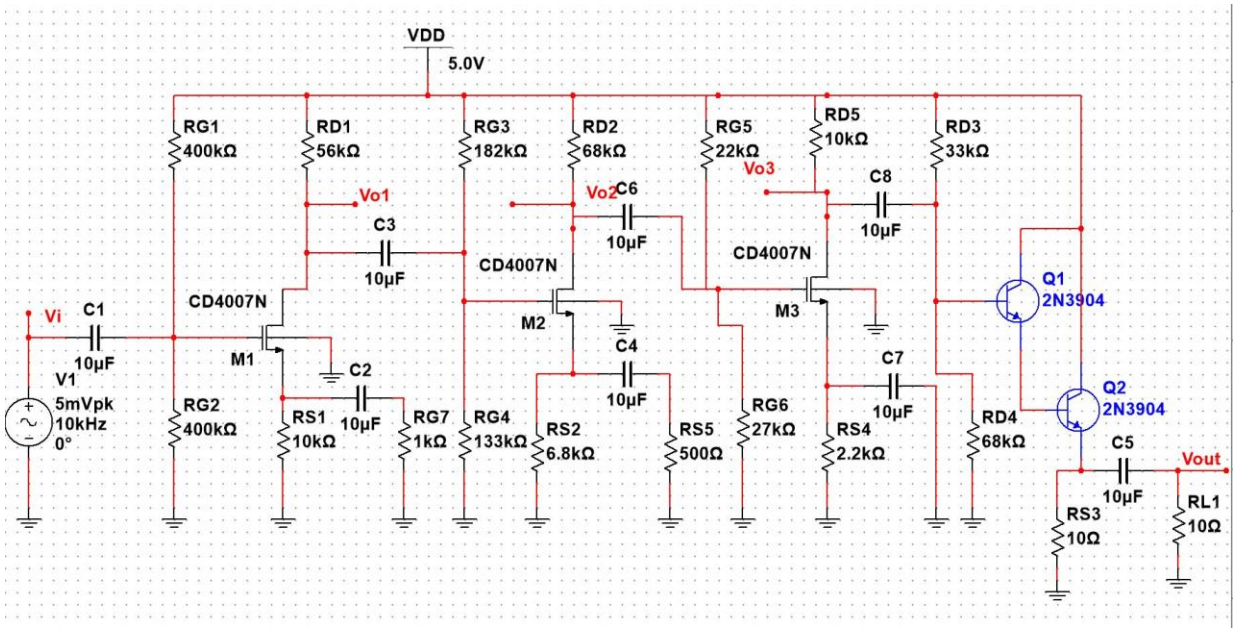
$G_m = \frac{g_m}{1 + g_m R_S}$

$A_{V_2} = 2$ $\quad A_V = -\frac{g_m R_D}{1 + g_m R_S}$

$g_m = 8.09 \times 10^{-3}$

$2 = \frac{(8.09 \times 10^{-3}) R_D}{1 + (8.09 \times 10^{-3}) 47K\Omega}$ $\quad 2 = \frac{8.09 \times 10^{-3} R_D}{(381.566)}$ $\quad R_D = 95330 \approx \boxed{100K\Omega}$

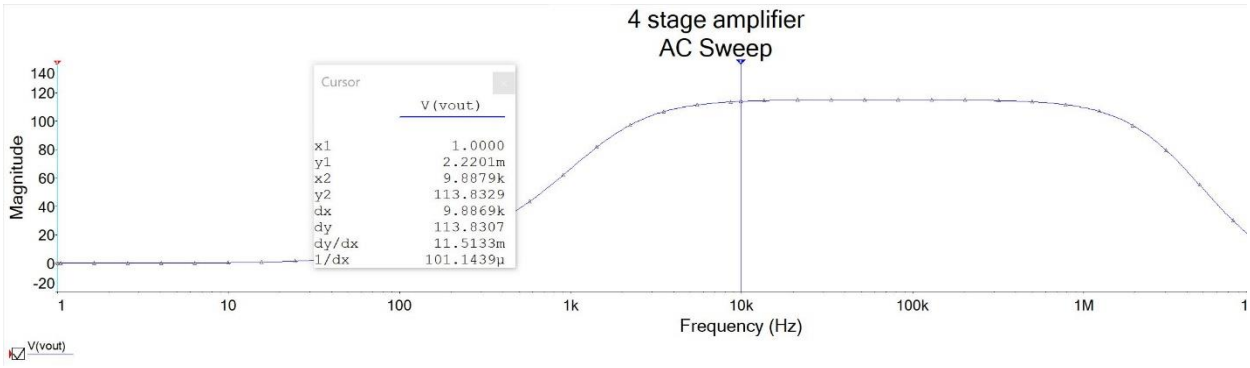
Simulations



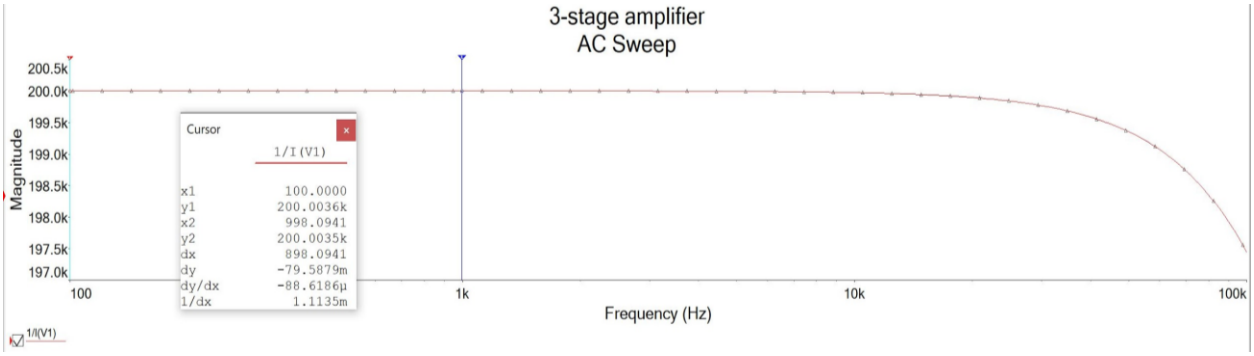
Schematic

	Variable	erating point va
1	V(vdd) - V(vo1) | V(VRD1)	3.65078
2	V(vdd) - V(vo2) | V(VRD2)	3.56219
3	V(vdd) - V(vo4) | V(VRD3)	1.91254
4	V(vo4) - V(0) | V(VRD4)	3.08746
5	V(vdd) - V(2) | V(VRG1)	2.50000
6	V(2) | V(VRG2)	2.50000
7	V(vdd) - V(3) | V(VRG3)	2.88889
8	V(3) | V(VRG4)	2.11111
9	V(vdd) - V(12) | V(VRG5)	2.24490
10	V(12) | V(VRG6)	2.75510
11	V(4) | V(VRG7)	0.00000e+000
12	V(5) | V(VRS1)	651.92553 m
13	V(7) | V(VRS2)	356.21879 m
14	V(10) | V(VRS3)	1.56266
15	V(14) - V(0) | V(VRS4)	595.34284 m

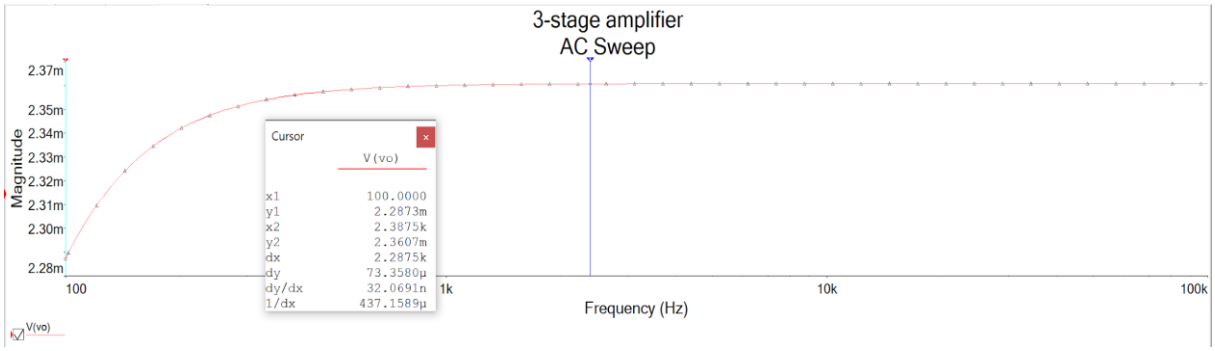
DC Operating Point



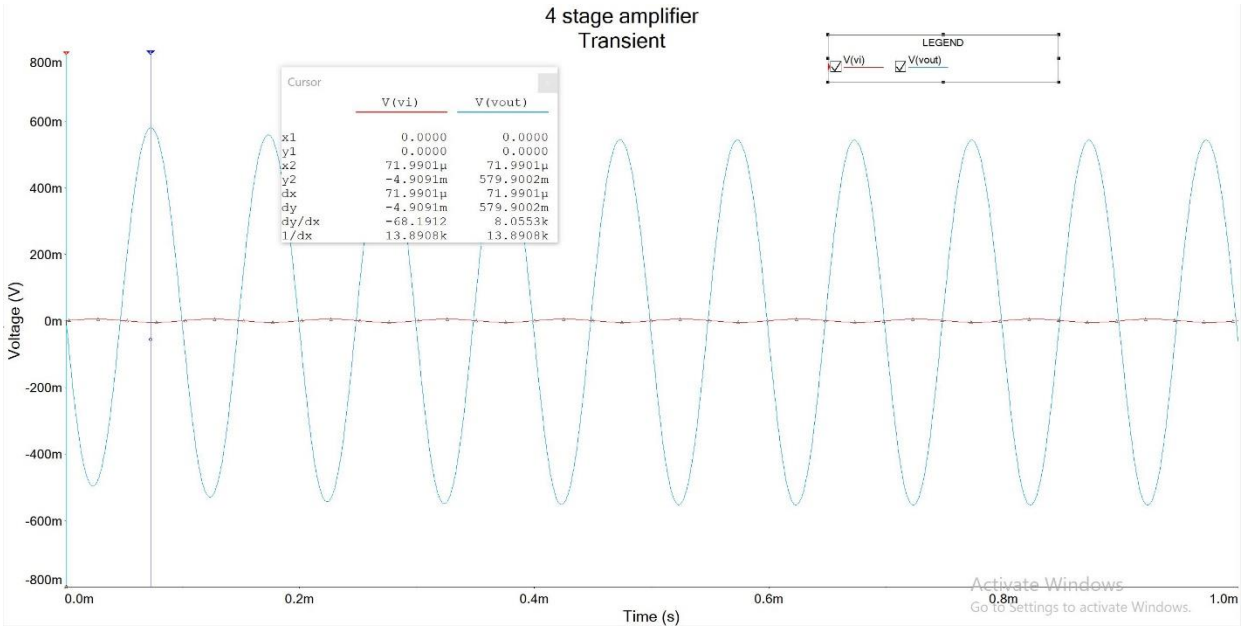
AC Sweep for Gain



AC Sweep for Input Resistance



AC Sweep for Output Resistance



Transient with V_i = 5mVsin(10,000t)

1	Fourier analysis for V(vout):					
2	DC component:	1.2532e-005				
3	No. Harmonics:	9				
4	THD:	1.55085 %				
5	Grid size:	256				
6	Interpolation Degree:	1				
7						
8	Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
9	0	0	1.2532e-005	0	2.26302e-005	0
10	1	10000	0.553771	-172.18	1	0
11	2	20000	0.00657764	94.2758	0.0118779	266.451
12	3	30000	0.00543696	-173.42	0.00981807	-1.2431
13	4	40000	0.000939296	101.661	0.00169618	273.836
14	5	50000	0.000211992	15.638	0.000382816	187.814

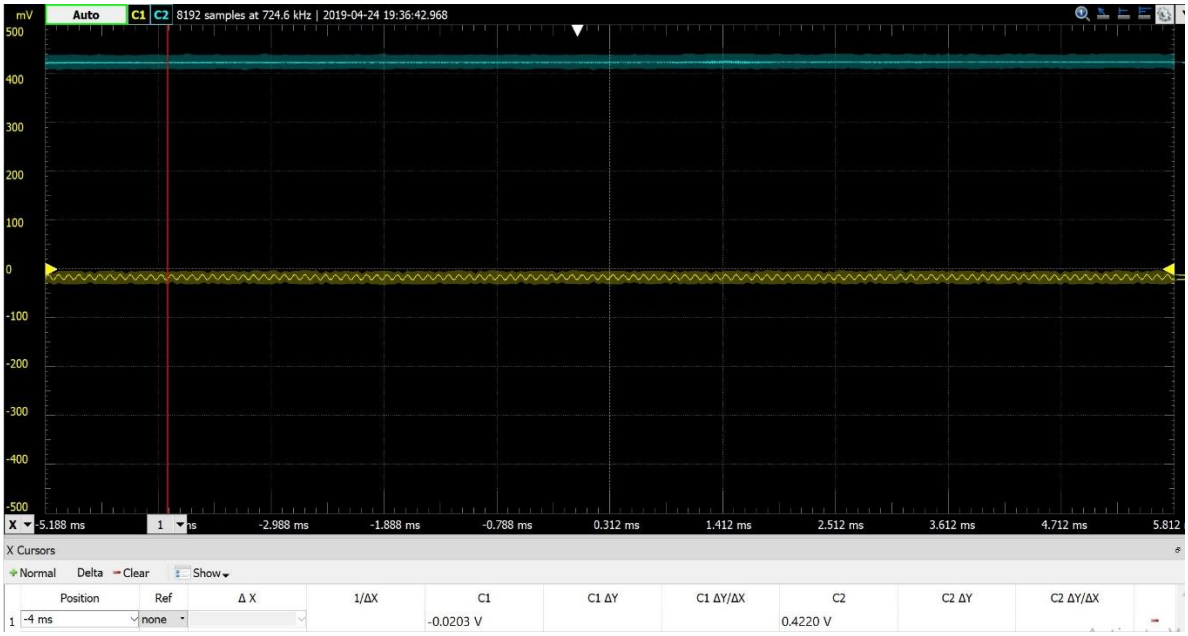
THD

Calculating Total Power dissipated:

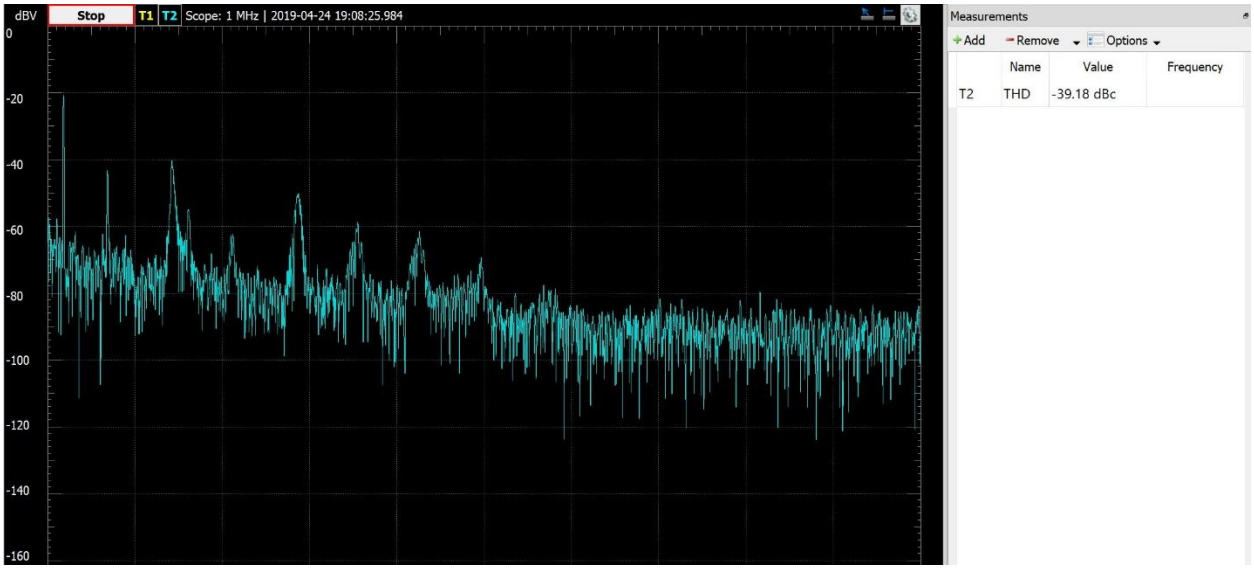
From the voltage across each resistor obtained using DC Operating point, we calculated the total power dissipated by finding power dissipated by each resistor using the formula, $P = V^2/R$ and adding them all together. By doing so, we obtained the total power dissipated.

Total power dissipated = 245 mW

Measurements



Transient



THD

Comparisons

Parameter	Requirement/Calculation	Simulation	Measurements
$\|A_V\|$	≥50	114	84.4
R_{in}	≥200kΩ	200.6 kΩ	200.6 kΩ
V_{out}	0.250 V	0.680 V	0.420 V
THD	≤-30 dB	-36.2 dB	-39.18 dB

Conclusion

We really enjoyed working on this project. It was quite a good experience for us to design a three-stage amplifier, even though it was really challenging. It helped understand about the MOSFET amplifiers better. The simulated values were able to satisfy the project requirements. The measurements part was the toughest part of this project. Measuring the scope for the circuit with so many components using the analog discovery 2 was a challenging process. Overall we were able to complete the project successfully.